PCT/JP2003/008973

Translation

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 310200641WO1	FOR FURTHER ACTION See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)	
International application No. PCT/JP2003/008973	International filing date (*day/month/year*) 15 July 2003 (15.07.2003)	Priority date (*day/month/year*) 22 July 2002 (22.07.2002)
International Patent Classification (IPC) or national classification and IPC G06F 13/16, 12/00		
Applicant RENESAS TECHNOLOGY CORP.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 9 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 9 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☒ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
15 July 2003 (15.07.2003)	02 November 2004 (02.11.2004)
Name and mailing address of the IPEA/JP Facsimile No.	Authorized officer Telephone No.

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/JP2003/008973

I. Basis of the report

1. With regard to the **elements** of the international application:*

☐ the international application as originally filed

☒ the description:
pages 1-43, as originally filed
pages _____, filed with the demand
pages _____, filed with the letter of _____

☒ the claims:
pages 5, 6, 12, 14, 19, 22, as originally filed
pages _____, as amended (together with any statement under Article 19
pages _____, filed with the demand
pages 1-4, 7-11, 13, 15-18, 20, 21, filed with the letter of 05 January 2004 (05.01.2004)

☒ the drawings:
pages 1-27, as originally filed
pages _____, filed with the demand
pages _____, filed with the letter of _____

☐ the sequence listing part of the description:
pages _____, as originally filed
pages _____, filed with the demand
pages _____, filed with the letter of _____

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

☐ the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

☐ contained in the international application in written form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☐ The amendments have resulted in the cancellation of:

☐ the description, pages _____

☐ the claims, Nos. _____

☐ the drawings, sheets/fig _____

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

* *Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rule 70.16 and 70.17).*

** *Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

IV. Lack of unity of invention

1. In response to the invitation to restrict or pay additional fees the applicant has:

- ☐ restricted the claims.
- ☐ paid additional fees.
- ☒ paid additional fees under protest.
- ☐ neither restricted nor paid additional fees.

2. ☐ This Authority found that the requirement of unity of invention is not complied with and chose, according to Rule 68.1, not to invite the applicant to restrict or pay additional fees.

3. This Authority considers that the requirement of unity of invention in accordance with Rules 13.1, 13.2 and 13.3 is

- ☒ complied with.
- ☐ not complied with for the following reasons:

4. Consequently, the following parts of the international application were the subject of international preliminary examination in establishing this report:

- ☒ all parts.
- ☐ the parts relating to claims Nos. _____.

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/JP 03/08973

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-22	YES
	Claims		NO
Inventive step (IS)	Claims		YES
	Claims	1-22	NO
Industrial applicability (IA)	Claims	1-22	YES
	Claims		NO

2. Citations and explanations

Document 1: US 5778419 A (Microunity Systems Engineering, Inc.), 07 July 1998, entire text, all drawings

Document 2: JP 2000-315185 A (Hitachi, Ltd.; Hitachi Video and Information System, Inc.), 14 November 2000, entire text, all drawings

Document 3: US 5794060 A (Microunity Systems Engineering, Inc.), 11 August 1998, fig. 16(a) and 16(b)

Document 4: JP 10-177427 A (Hitachi, Ltd.), 30 June 1998, entire text, all drawings

Document 5: JP 2000-148656 A (Mitsubishi Electric Corp.), 30 May 2000, paragraphs [0071] to [0086] and fig. 7-10

Document 6: JP 2001-14840 A (NEC Corp.), 19 January 2001, entire text, all drawings

Document 7: JP 10-136034 A (Ascom Tech AG), 22 May 1998, entire text, all drawings

Document 8: JP 11-88442 A (Yokogawa Electric Corp.), 30 March 1999, entire text, all drawings

Document 9: JP 2002-7308 A (NEC Corp.), 11 January 2002, entire text, all drawings

Document 10: JP 2001-156621 A (Toshiba Corp.), 08 June 2001, entire text, all drawings

Claims 1-3

The invention that is set forth in claims 1-3 does not involve an inventive step in the light of documents 1, 2, 9 and 10.

Document 1 discloses a memory chip wherein in response to a packet that has been synchronized with the clock and received via the input port, either a response signal that is generated by an internal circuit or the aforementioned packet that is received via the input port is output via the output port, and the packet and the clock are input and output via different terminals (fig. 1, elements 113, 114, 123 and 124).

Document 2 discloses semiconductor memory wherein in response to a command, an address or data that has been synchronized with the clock and received via the input port, either read data that is generated by an internal circuit or the aforementioned data that is received via the input port is output via the output port, and the clock and the data are input and output via different terminals (fig. 1, elements 200, 300, 201 and 301).

Document 9 discloses an invention that is configured with one-to-one connections between the storage elements and between the memory control elements and the storage elements, wherein each element inputs and outputs the address signals, the clock signals, the data signals and the request control signals via different terminals.

Document 10 discloses an invention that is configured with one-to-one connections between the memory LSIs and between the controller LSIs and the memory LSIs, and, with the exception of an example wherein each memory LSI transmits and receives the data, the addresses and the commands in a single integrated package (paragraphs [0230] to [0240] and fig. 45), presents examples wherein the transmission paths for the data, the address signals and

the control signals are separate (paragraphs [0183] to [0186] and [0190], and fig. 41).

It would be easy for a person skilled in the art to configure the memory that is disclosed in document 1 or document 2 so that not only the clock, but also the control signals, the address signals and the data signals are input and output via different terminals in the light of documents 9 and 10.

Claims 4-6

The invention that is set forth in claims 4-6 does not involve an inventive step in the light of documents 1, 9 and 10. The skew of the signals is adjusted by means of a clock that is regenerated by an internal PLL in the memory chip that is disclosed in document 1 (refer to fig. 7).

Claims 7 and 8

The invention that is set forth in claims 7 and 8 does not involve an inventive step in the light of documents 1, 2, 8 and 9. In addition to the disclosures pertaining to claims 1-3 above, the inventions that are disclosed in documents 1 and 2 also are configured with one-to-one connections between the corresponding terminals of the plurality of memory chips and between the corresponding terminals of the memory chips and the host device (500) (document 1) or the controller (2) (document 2).

Claim 9

The invention that is set forth in claim 9 does not involve an inventive step in the light of documents 1, 9 and 10, for the same reasons as presented in relation to claims 4-6 above.

Claims 10-12

The invention that is set forth in claims 10-12 does not involve an inventive step in the light of documents 1, 2, 9 and 10. In addition to the disclosures pertaining to claims 1-3 above, the inventions that are disclosed in documents 1 and 2 are also configured so that among the plurality of memory means, the output terminals of the memory means in the preceding stage and the corresponding input terminals of the memory means in the following stage are connected in a cascade configuration in order to form a ring bus with the host device (500) (document 1) or the controller (2) (document 2) (refer to document 1, fig. 5 and document 2, fig. 3).

Claims 13 and 14

The invention that is set forth in claims 13 and 14 does not involve an inventive step in the light of documents 1, 9 and 10 for the same reasons as presented in relation to claims 4-6 above.

Claims 15, 17 and 18

The invention that is set forth in claims 15 and 17 does not involve an inventive step in the light of documents 1-3, 9 and 10. It would be easy for a person skilled in the art to configure a plurality of channels by providing a plurality of ring busses, as disclosed in document 3 (fig. 16(a) and 16(b)).

Claim 16

The invention that is set forth in claim 16 does not involve an inventive step in the light of documents 1-4, 9 and 10. Document 4 (fig. 12 and paragraph [0101]) discloses the feature of configuring address/command lines for each system by branching the address/command line from the memory controller before the point where it is

connected to the plurality of memory means that constitute the initial stages. Consequently, it would be easy for a person skilled in the art to configure address/command lines for each channel by branching the address/command line from the memory controller before the point where it is connected to the memory means in the initial stage of each channel when configuring a plurality of channels by providing a plurality of ring busses.

Claim 19

The invention that is set forth in claim 19 does not involve an inventive step in the light of documents 1-5, 9 and 10. Document 5 (paragraphs [0071] to [0086] and fig. 7-10) discloses the feature of mounting memory upon both surfaces of a substrate and configuring a ring bus by connecting the busses on both sides of the substrate via through holes. It would be easy for a person skilled in the art to conceive of the items that are set forth in claim 19 in the light of said disclosure.

Claim 20

The invention that is set forth in claim 20 does not involve an inventive step in the light of documents 1, 2, 6, 9 and 10. Document 6 discloses the feature of providing a prefetch command for reading data out from the memory cell array to the buffer, and a buffer read command for outputting the data from the buffer to the external output terminal. Consequently, it would be easy to provide a prefetch command and a buffer read command to the response buffer (404) in the invention that is disclosed in document 1.

Claim 21

The invention that is set forth in claim 21 does not involve an inventive step in the light of documents 1, 2,

6, 9 and 10. The feature wherein data is autonomously read into the memory means from the light buffer is well known; therefore, it is not especially difficult to configure so that data is autonomously read into the memory cells from the light buffer in the invention that is disclosed in document 1.

Claim 22

The invention that is set forth in claim 22 does not involve an inventive step in the light of documents 1, 2 and 7-10. Documents 7 and 8 disclose data transmission formats wherein n number of transmission lines among the m number of transmission lines are switched to a different level.